**ELEC5566M-FPGA Design for System-on-chip**

Unit 2: Written Assignment – Digital Lock

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**Abstract**

A digital lock was made via Verilog and state mechanisms, and a test bench was used for verification and simulation to prove the viability of the system. The report contains an introduction to the use of digital locks, status tables and diagrams, simulation, discussion and conclusion.

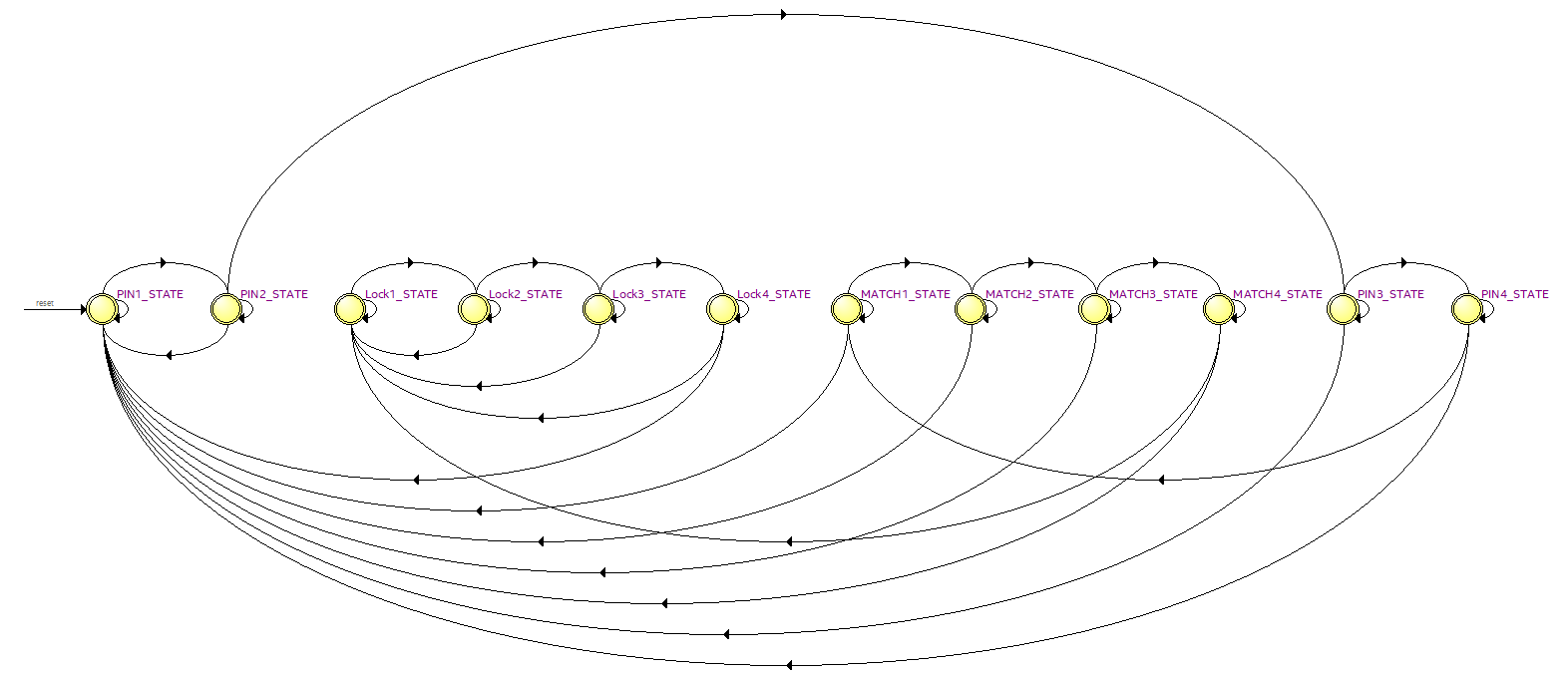
**Introduction**

The goal of the written assignment is to create a simple digital lock using Verilog and a state machine.

At the initial stage the system is the unlocked state and the user needs to make the system into a locked state by inputting the same key sequence twice. Firstly, during the PIN setting stage, the user needs to press four key buttons and the sequence in which the key buttons are pressed will be used as the PIN code and the first set of key button sequence. Then, during the matching stage, the user needs to press the four key buttons again, and the pressed key buttons need to be in the same sequence as the first set of pressed key buttons. If the sequence of the buttons matches successfully, the system will enter the locked state and the LOCKED indicator output will be marked high. If it fails, the system will re-enter the PIN setting stage and the error indicator output will be marked high.

When the system is the locked state, the user is able to return the system to the unlocked state by inputting the same key sequence as the PIN code. If an incorrect key sequence is input, the system should remain locked state. In addition, if the user presses the ‘reset’ button, it will reset the system and bring it back to the initial PIN code setting stage.

Note: The system does not allow repeated button presses when inputting a set of button sequences, otherwise the EROE indicator will also become ‘High’.

**State table and diagram**

**Figure 1:** The state diagram

In Verilog, a state diagram is made using the state machine, as shown in Figure 1. The digital lock requires 12 times pressing the key button to complete a lock and unlock, thus setting 12 states. The 12 states can be divided into 3 parts, the first 4 states are the PIN setting stage, the middle 4 states are the matching stage and the last 4 states are the decoding stage.

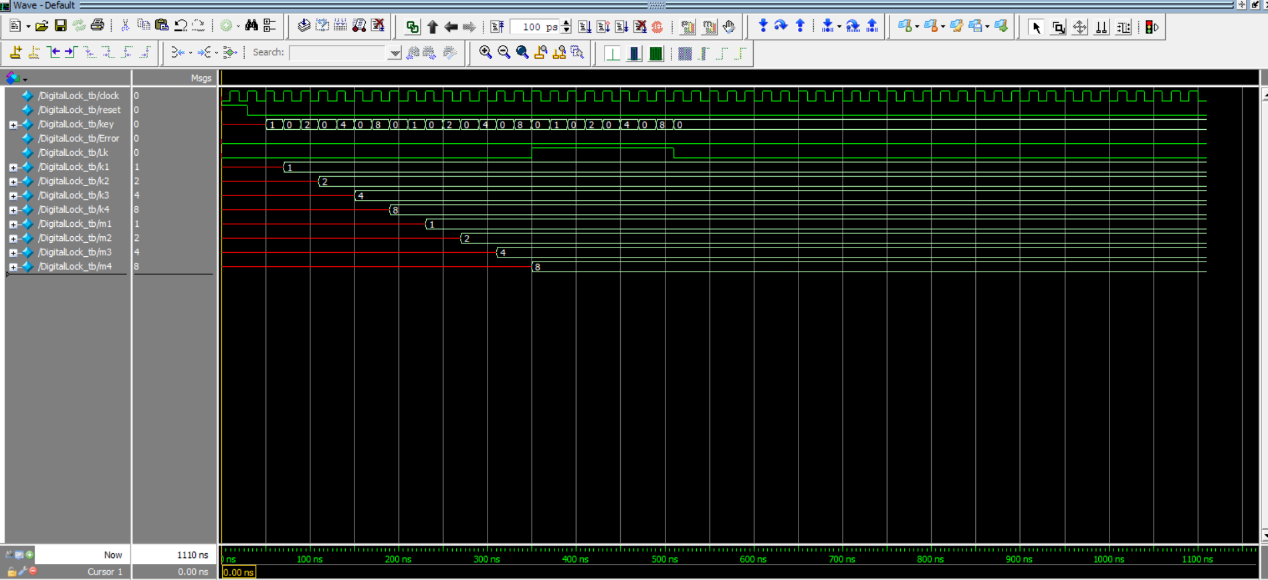
**Table 1:** The state table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Next State | | Output Error | | Output |
| Present State | F | T | F | T | Lk |
| PIN1\_STATE | PIN1\_STATE | PIN2\_STATE | 0 | 0 | 0 |
| PIN2\_STATE | PIN1\_STATE | PIN3\_STATE | 0 | 0 | 0 |
| PIN3\_STATE | PIN1\_STATE | PIN4\_STATE | 0 | 0 | 0 |
| PIN4\_STATE | PIN1\_STATE | MATCH1\_STATE | 0 | 0 | 0 |
| MATCH1\_STATE | PIN1\_STATE | MATCH2\_STATE | 1 | 0 | 0 |
| MATCH2\_STATE | PIN1\_STATE | MATCH3\_STATE | 1 | 0 | 0 |
| MATCH3\_STATE | PIN1\_STATE | MATCH4\_STATE | 1 | 0 | 0 |
| MATCH4\_STATE | PIN1\_STATE | Lock1\_STATE | 1 | 0 | 0 |
| Lock1\_STATE | Lock1\_STATE | Lock2\_STATE | 1 | 0 | 1 |
| Lock2\_STATE | Lock1\_STATE | Lock2\_STATE | 1 | 0 | 1 |
| Lock3\_STATE | Lock1\_STATE | Lock4\_STATE | 1 | 0 | 1 |
| Lock4\_STATE | Lock1\_STATE | PIN1\_STATE | 1 | 0 | 1 |

A simple state table has been created based on the state diagram. ‘T’ and ‘F’ in the table are the conditions to be judged. Since the judgement conditions are different for each state, ‘T’ and ‘F’ are used instead.

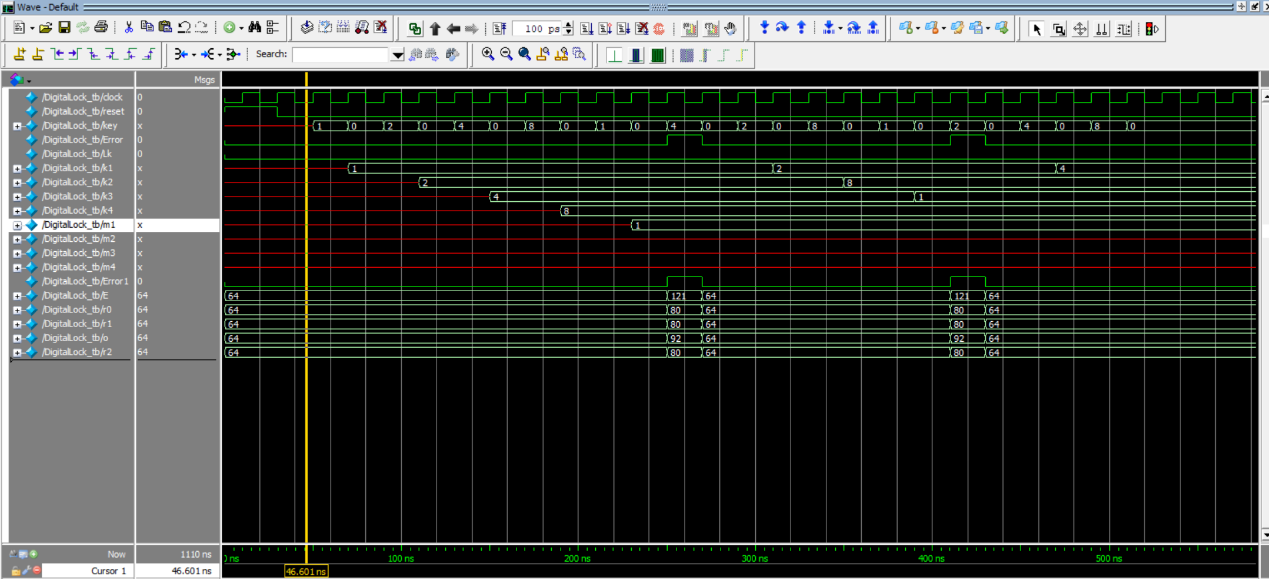
The table shows that when condition ‘T’ is reached, it can go to the next stage. Only during the matching and decoding phase will it determine if the wrong key button has been inputted. During the decoding phase, the LOCKED (Lk) indicator remains high.

**Simulation**



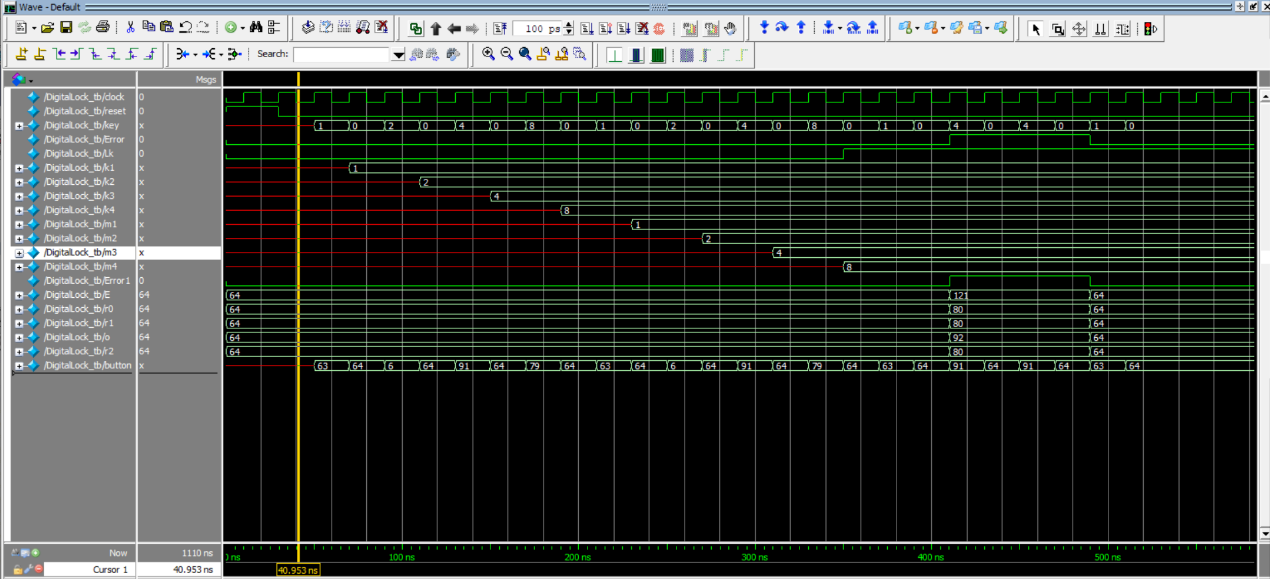
**Figure 2:** The simulation of the Unlocked state and Locked state

Figure 2 shows a simulation of the basic unlocked and locked states. By inputting the same code three times, it can be seen that ‘Lk’ goes ‘High’ after the second set of buttons is input, as a lock state. Then, after the third set of buttons is input, ‘Lk’ returns to a ‘Low’ as an unlocked state. Output ‘k’ and ‘m’ to determine which state the system is in.



**Figure 3:** The simulation of ERROR indicator

By changing the sequence of buttons in the matching stage, it can see that the ERROR indicator becomes ‘High’. When the ‘ERROR’ indicator is ‘High’, ‘E’, ‘r’, ‘r’, ‘o’ and ‘r’ are output on respectively the five 7-segment displays. When the ERROR indicator is ‘Low’, a '-' is output simultaneously on the five 7-segment displays. After the ERROE indicator becomes ‘High’, it can be seen that the system returns to the PIN setting stage and also displays an Error when a repeat button is input.



**Figure 4:** The simulation of Locke state

As in Figure 4, in the locked state, if the user inputs the wrong button sequence, you can see that the system is still locked state. To show which key is pressed on a 7-segment display, ‘KeyTo7Segment’ is added, which displays 0 to 3 on a 7-segment display when the user presses a key, representing respectively the four key buttons.

**Discussion & Conclusion**

Through simulation, the basic functions of the digital lock are proven to be available. Normally, however, the function of the digital lock should be allowed to operate only after the user has pressed the button and released it, in order to prevent the user from pressing the correct button but holding it down for so long that the system enters it twice and considers it an error. Therefore, a new code system needs to be added to execute the function when the user releases the button.

In addition, a condition to judge whether the first three buttons are pressed has been added to prevent users from pressing repeated buttons. However, the system can operate after adding this judgement, but cannot create a status diagram. A status diagram is created when judging whether the first two buttons are pressed. Thus, the state machine may not be able to handle overly complex judgements.

A timer has also been programmed to limit the amount of time the user has to input buttons. However, similarly, when the timer is added to the system, the system can operate but cannot create a status diagram.

Overall, the digital lock for this state machine is operational but not perfect at the moment. An in-depth review of state machines is also needed.